WHAT IS CLAIMED IS:

1. An interconnect provided on an insulator base, the interconnect having a three-layer structure composed of a barrier film for metal diffusion provided on the insulator base instead of being buried in the insulator base, a metal seed layer provided on the barrier film for metal diffusion, and a metal conductive layer provided on the metal seed layer.

2. The interconnect according to claim 1, wherein the barrier film for metal diffusion has an externally exposed peripheral surface, the metal seed layer has a top surface and a peripheral surface, and the metal conductive layer has a peripheral portion formed on the a peripheral surface of the metal seed layer and has a peripheral surface flush with the peripheral surface of the barrier film for metal diffusion and surrounds the top surface and peripheral surface of the metal seed layer.

3. The interconnect according to claim 1, wherein the barrier film for metal diffusion has an externally exposed peripheral surface, the metal seed layer has a top surface and a peripheral surface, and the metal conductive layer has a peripheral surface projecting outward from the peripheral surface of the barrier film for metal diffusion and surrounds the top surface and peripheral surface of the metal seed layer.

4. The interconnect according to claim 1, wherein

the barrier film for metal diffusion has an externally exposed peripheral surface, the metal seed layer has a top surface and an externally exposed peripheral surface, the metal conductive layer has an externally exposed peripheral surface and is deposited on the top surface of the metal seed layer, and the peripheral surface of the metal conductive layer, the peripheral surface of the metal seed layer, and the peripheral surface of the barrier film for metal diffusion are flushed with one another.

5. An interconnect forming method comprising:

a step of forming a barrier film for metal diffusion on an insulator base;

a step of selectively forming a metal seed layer on the barrier film for metal diffusion; and

a step of selectively forming a metal conductive layer on the metal seed layer using an electroplating process.

6. An interconnect forming method comprising:

a step of forming a barrier film for metal diffusion on an insulator base;

a step of selectively forming a metal seed layer on the barrier film for metal diffusion using an electroless plating process;

a step of selectively forming a metal conductive layer on the metal seed layer using an electroplating process; and

a step of etching the barrier film for metal diffusion using the metal conductive layer as a mask.

7. An interconnect forming method comprising:

a step of forming a barrier film for metal diffusion on an insulator base;

a step of selectively forming a metal seed layer on the barrier film for metal diffusion using an electroless plating process;

a step of etching the barrier film for metal diffusion using the metal seed layer as a mask; and

a step of selectively forming a metal conductive layer on the metal seed layer using an electroplating process.

8. The interconnect forming method according to claim 5, wherein the insulator base has a substrate and an underlying insulator film provided on the substrate.

9. The interconnect forming method according to claim 5, further comprising a step of carrying out annealing after the metal seed layer has been formed to reduce film stress that may occur in the metal seed layer.

10. The interconnect forming method according to claim 5, wherein the step of selectively forming the metal seed layer on the barrier film for metal diffusion using the electroless plating process uses a mask composed of a photosensitive resin and having a trench shaped so as to correspond to an area in which

the metal seed layer is formed, to execute the electroless plating process to form the metal seed layer on the barrier film for metal diffusion exposed from this trench.

11. A thin film transistor comprising:

a semiconductor layer having a channel area as well as a source area and a drain area provided at respective sides of the channel area;

a gate insulator film provided on the semiconductor layer; and

a gate electrode provided on the gate insulator film;

wherein the gate electrode has a three-layer structure composed of a barrier film for metal diffusion provided on the gate insulator film instead of being buried in the gate insulator film, a metal seed layer provided on the barrier film for metal diffusion, and a metal conductive layer provided on the metal seed layer.

12. A thin film transistor comprising:

a semiconductor layer having a channel area as well as a source area and a drain area provided at respective sides of the channel area;

a gate insulator film provided on the semiconductor layer;

a gate electrode provided on the gate insulator film opposite the channel area;

a source electrode electrically connected to the source area; and

a drain electrode electrically connected to the drain area

wherein at least one of the gate electrode, the source electrode, and the drain electrode has a three-layer structure composed of a barrier film for metal diffusion, a metal seed layer provided on the barrier film for metal diffusion, and a metal conductive layer provided on the metal seed layer.

13. A display device comprising a plurality of thin film transistors arranged in matrix form, wherein each of the plurality of thin film transistors is the thin film transistor according to claim 11 or 12.

14. A display device comprising a plurality of thin film transistors arranged in matrix form, and a plurality of scan lines and a plurality of signal lines which are used to drive the thin film transistors

wherein at least one of the set of scan lines and the set of signal lines has a three-layer structure composed of a barrier film for metal diffusion, a metal seed layer provided on the barrier film for metal diffusion, and a metal conductive layer provided on the metal seed layer.